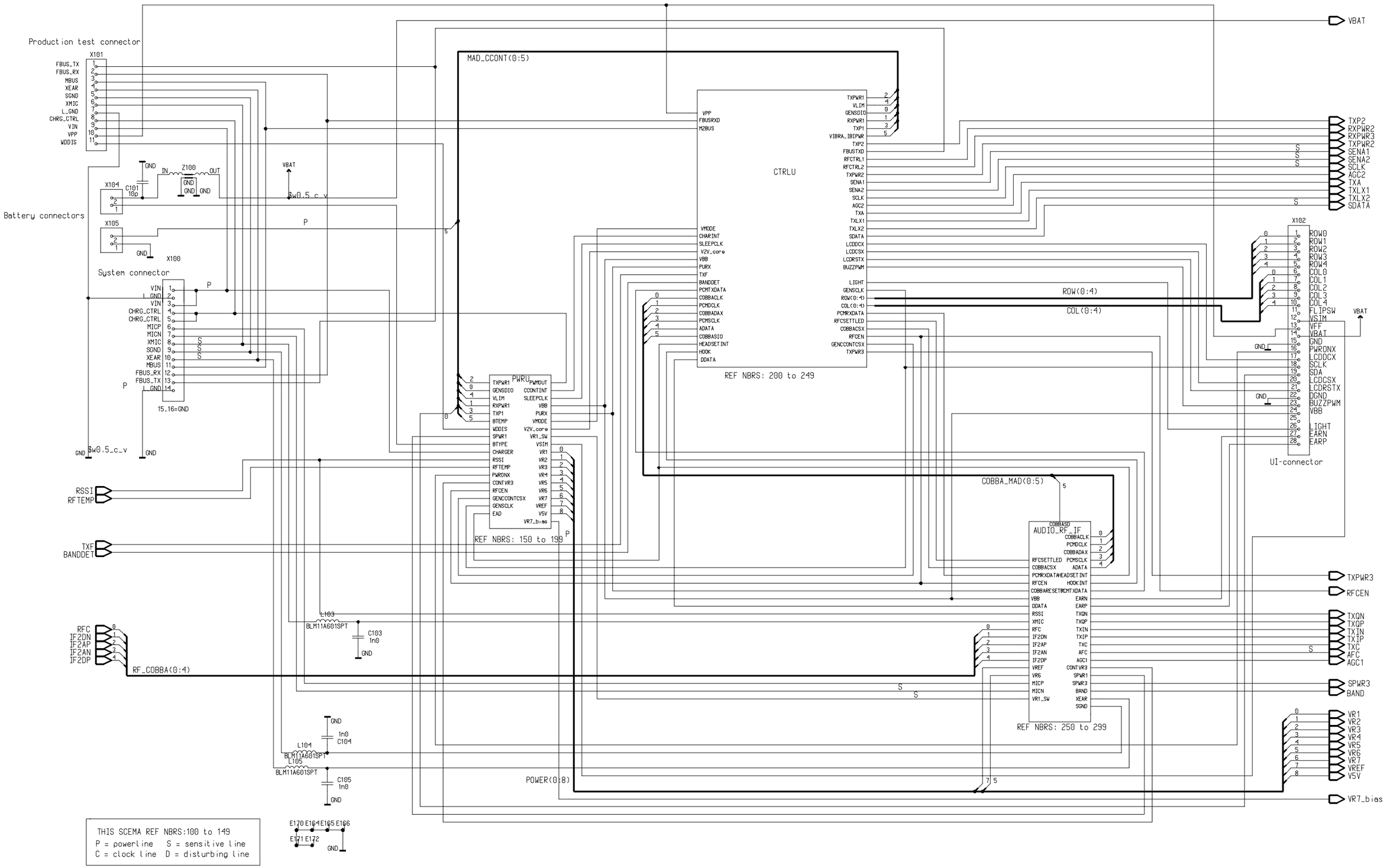
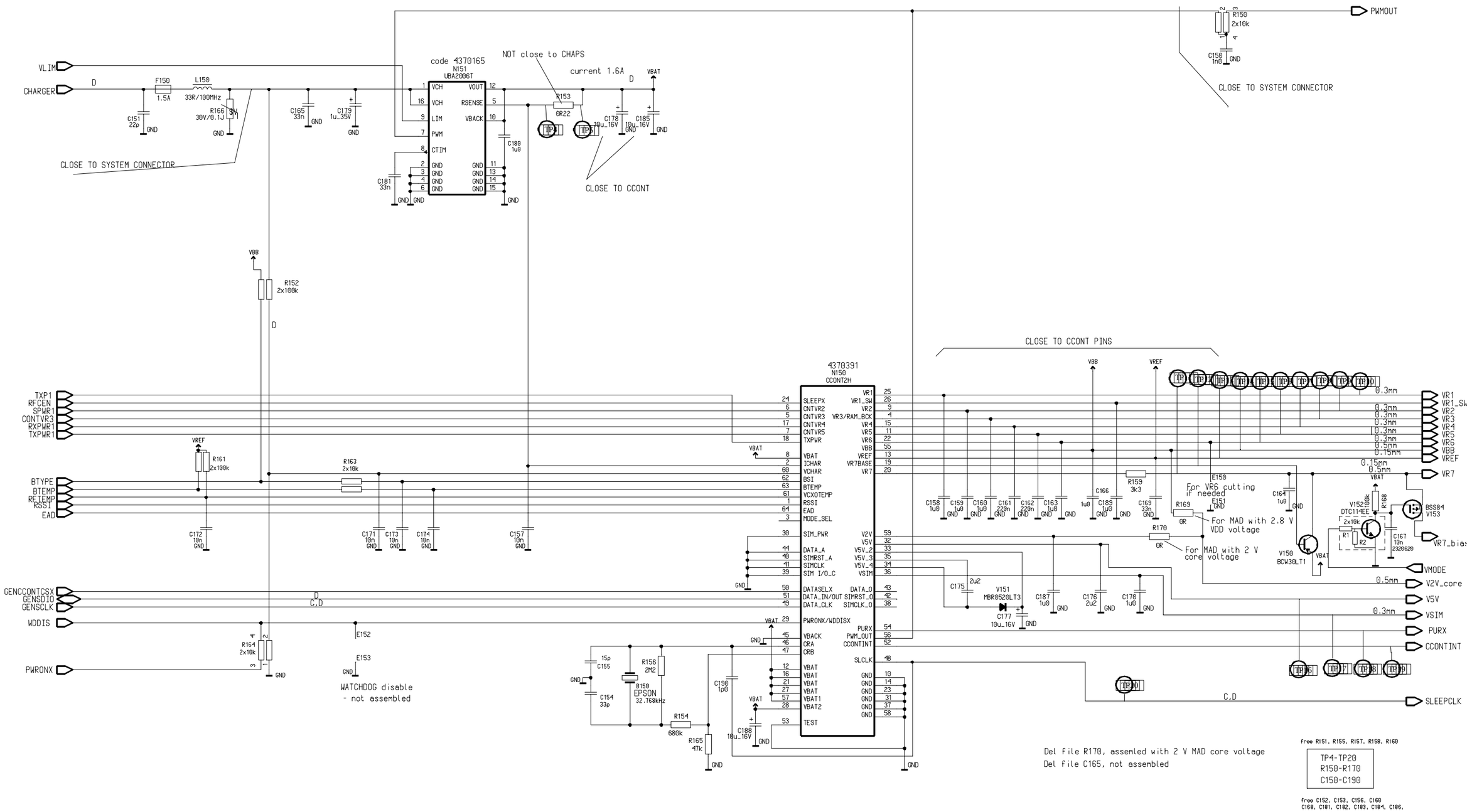
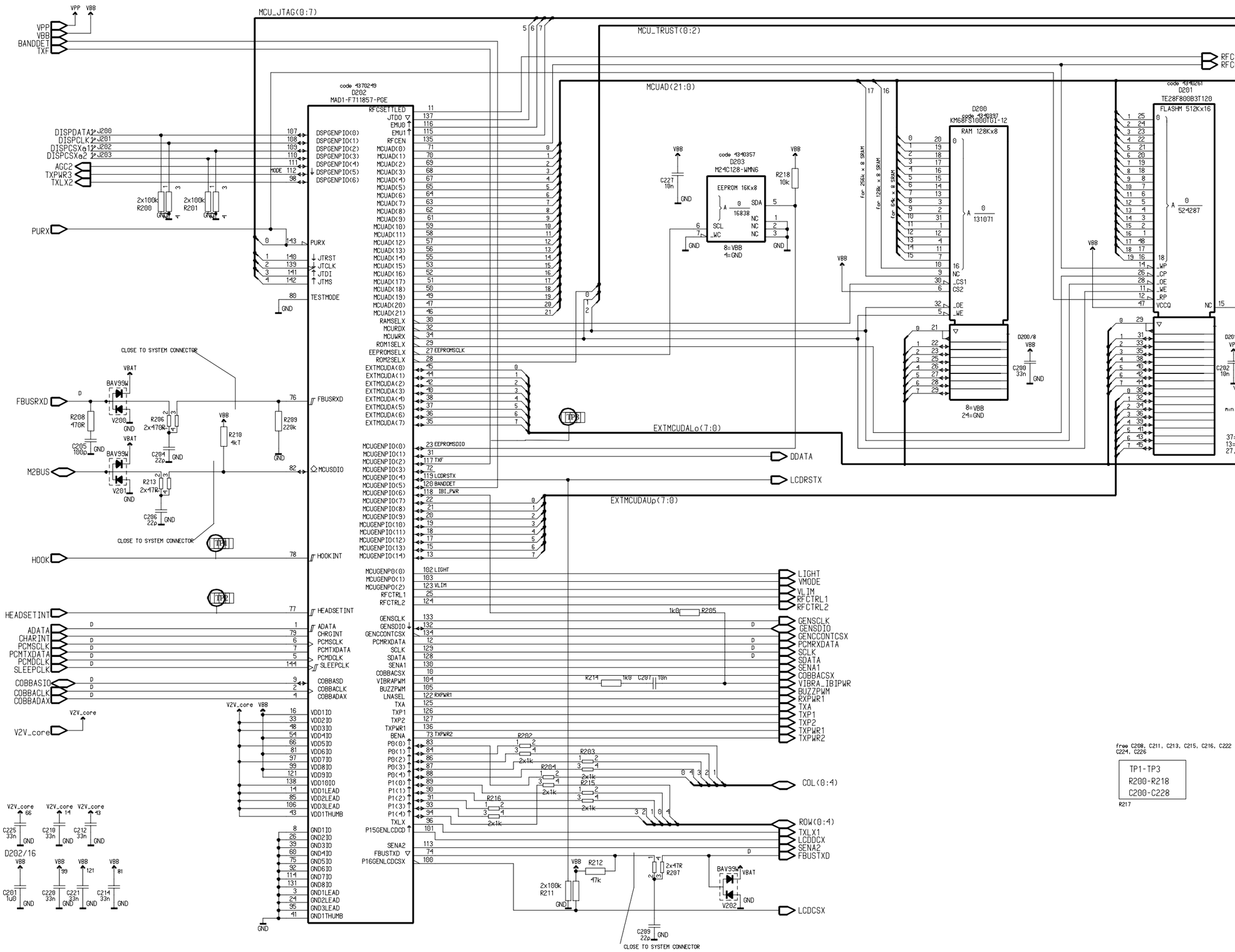
Circuit Diagram of System Blocks (Version 04.27 Edit 204)



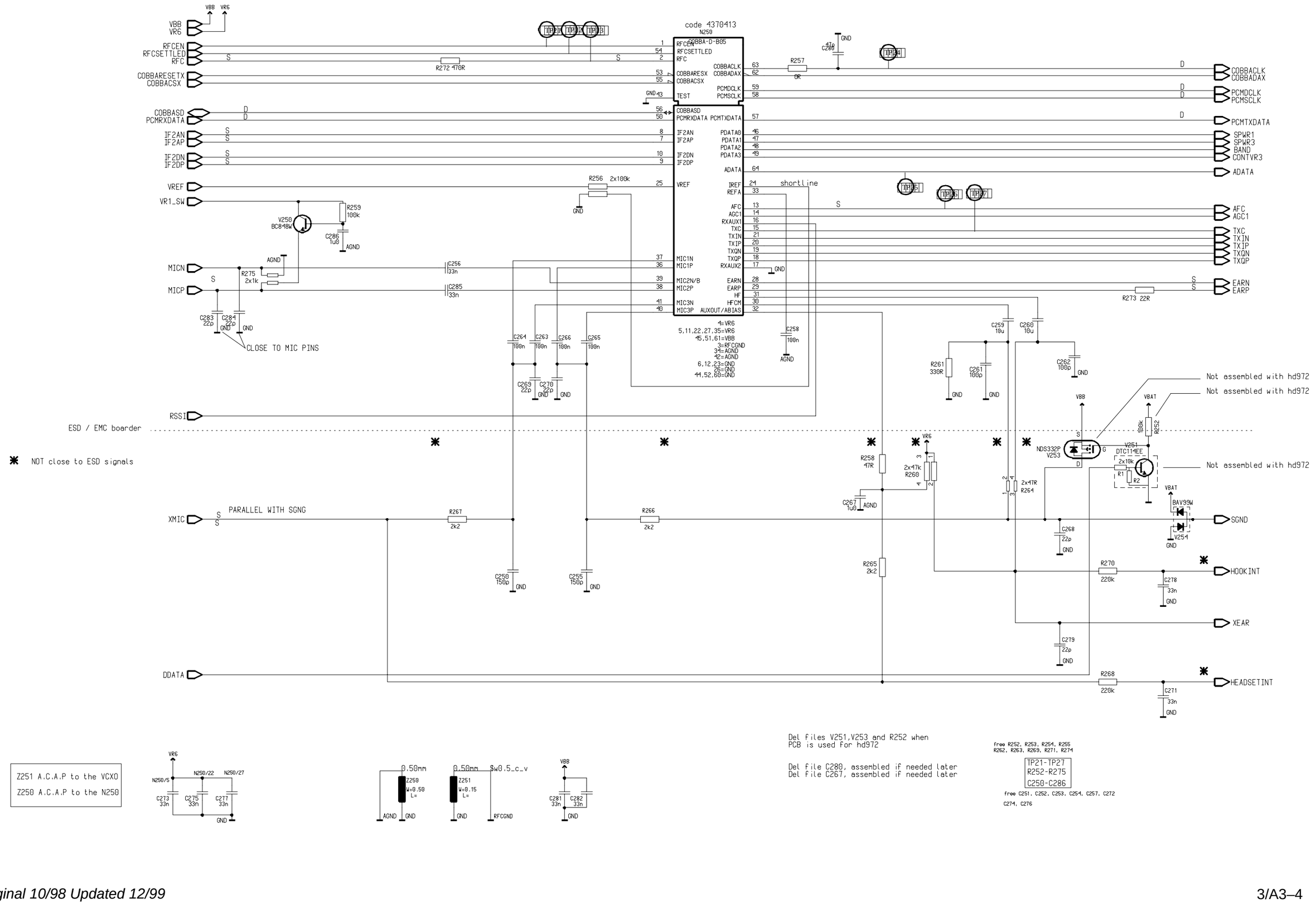
Circuit Diagram of Power Supply (Version 04.27 Edit 300)



Circuit Diagram of CTRLU Block (Version 04.27 Edit 293)



Circuit Diagram of Audio (Version 04.27 Edit 241)



Z251 A.C.A.P to the VCXO

Z250 A.C.A.P to the N250

Del files V251,V253 and R252 when PCB is used for hd972

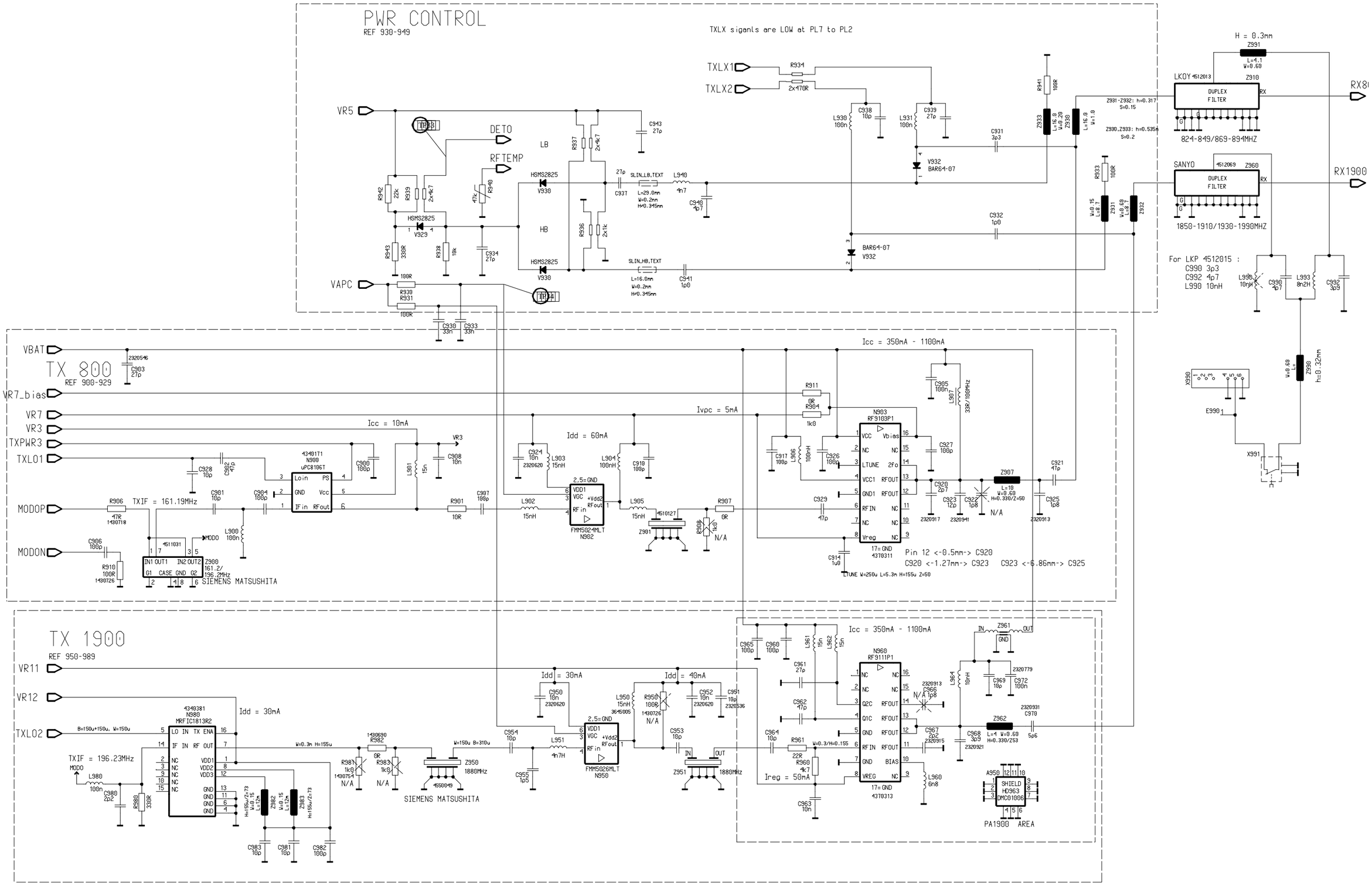
Del file C280, assembled if needed later
Del file C267, assembled if needed later

free R252, R253, R254, R255 R262, R263, R269, R271, R274

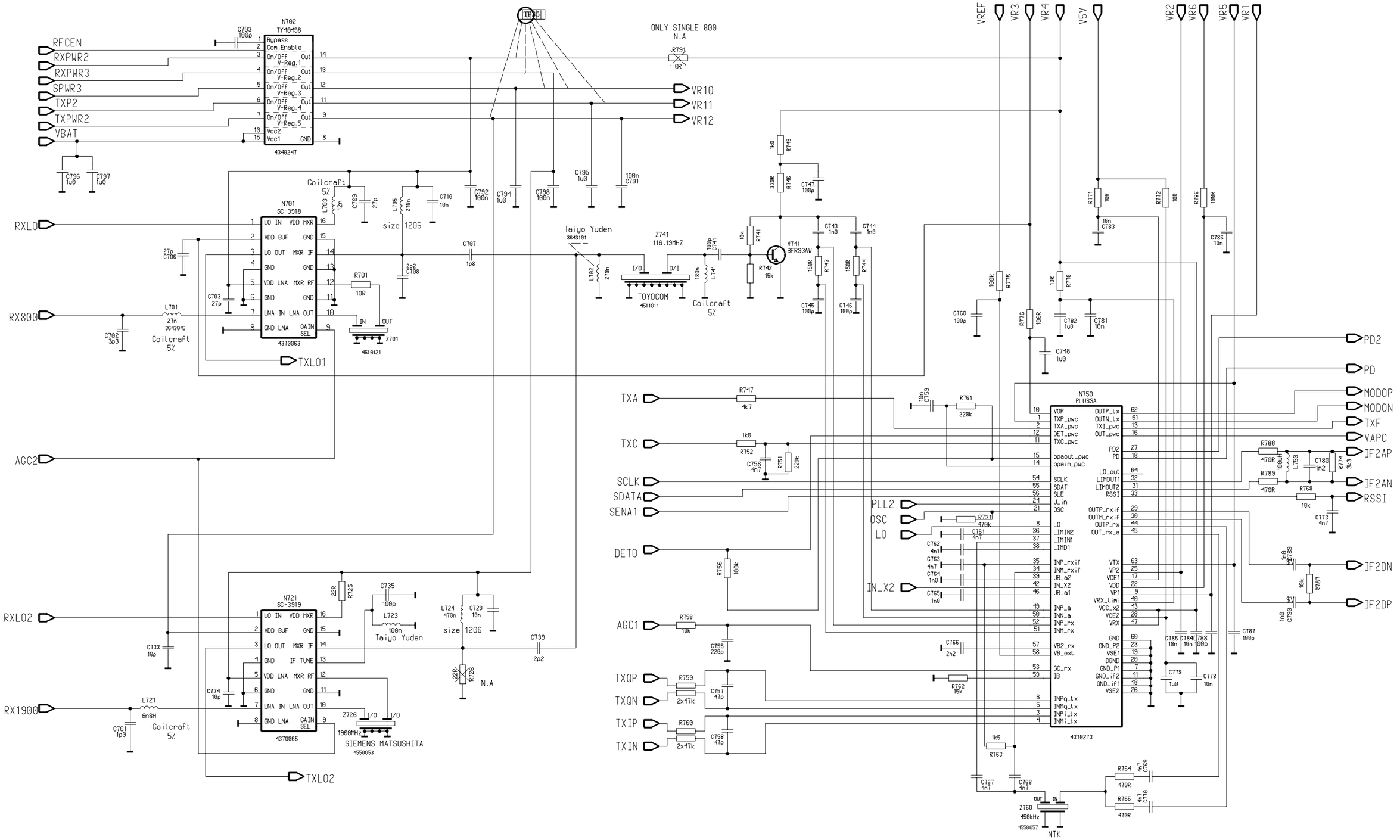
TP21-TP27
R252-R275
C250-C286

free C251, C252, C253, C254, C257, C272 C274, C276

Circuit Diagram of Transmitter (Version 04.27 Edit 583)



Circuit Diagram of Receiver (Version 04.27 Edit 131)



Circuit Diagram of Synthesizer (Version 04.27 Edit 157)

VR2
PD2
PLL2
RXLO
VR3
BAND
PD
VR1
AFC
LO
IN_X2
OSC
VR10
SCLK
SDATA
SENA2
BANDDET
RFC
RXLO2
V5V

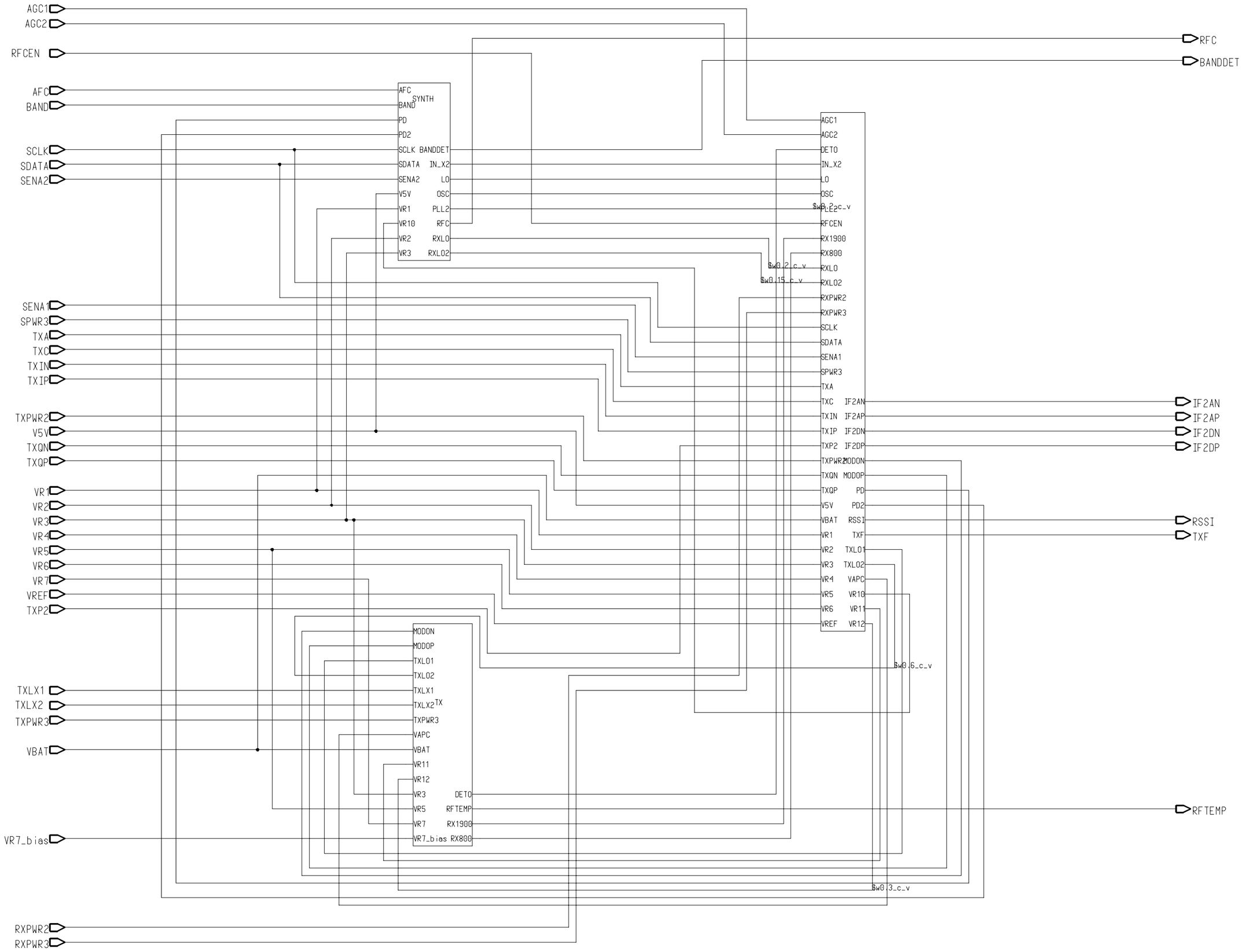
R822 10R
C824 10u_16V
C825 100p
G820 450121
URAA8-D02A
C821 1p0
0.20mm Z820 L=24m W=0.20
Z821 L=28m W=0.20 0.20mm
C830 1n0
R830 33k
C831 4n7
R832 220R
C833 150p
R833 10R
C834 150p
R831 10R
R821 22R
R823 22R

R851 100R
R843 100R
C845 1u0
C855 1u0
R841 10k
L840 100nH
33p C840
G850 450165
NKG3076A
19.44MHz
C854 3p3
C843 6p8
100p C842
V840 BFR93AW
L841 100nH
C841 220p
R850 10k
C850 100n
15k R840
1k0 R842
C844 1n0

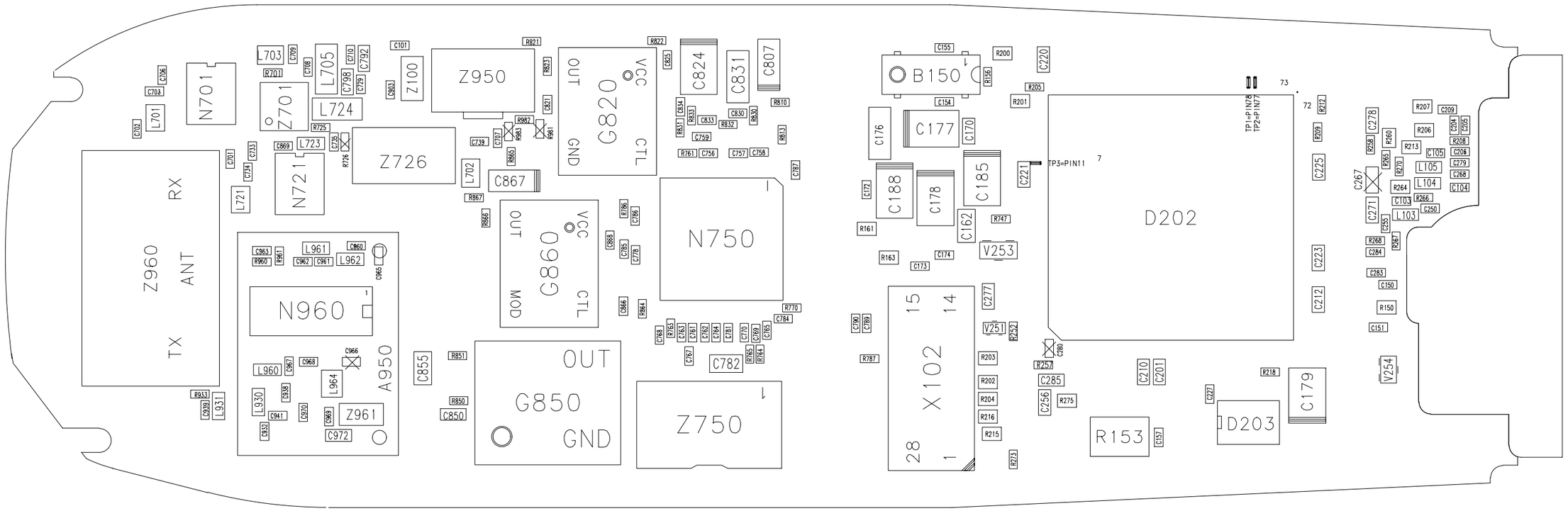
VB1
R804 100k
C815 1n0
D801 TC7S00F
5=VB1 3=GND
R805 1k0
BA532 V801
C805 100p
BB135 V802
R806 10k
1SV239 V803
R802 1k0
R803 1k0
L801 47nH
18p C806
C891 1n0
10k R891
C892 10n
C893 1n0
5k6 R808
C808 15p
C809 10p
33R R809
C811 2p2
100R R810
2k2 R807
10R R814
C816 1p0
C807 4u7_10V
C818 100p
V800 BFM505
10k R812
22k R811
1k0 R813
V800 BFM505
Murata LQN21A, 2?, Q40/200MHz, vertical coil

1n0 C851
R865 10R
C867 4u7_16V
C868 100p
R880 10R
R893 1k0
C881 1n0
R886 5k6
C898 100p
C882 4u7_10V
C886 1n0
C885 1n0
C887 1u0
R881 100R
N880 UMA1021M 4340237
C860 450117
URAA8-D04A
3k3 R861
100R R862
10R R864
C865 1n0
C864 150p
C866 150p
R867 10R
R866 10R
C860 1n0
R860 10k
C861 18n 2420017
Matsushita Film Chip Capacitor ECHU1C183JB5 (18n)
Z880 L=16.0 0.15mm W=0.15 B: 150mm+150mm
R855 100R
C856 1u0
R852 10k
C853 1n0
V850 BC848W
3u9H L850
C858 1n0
15k R853
1k0 R854
C857 220p
0.15mm Z881 L=25.0 W=0.15 B: 150mm+150mm
C869 2p7
R894 100k Assembled only single band phon
R895 100k Assembled only dual band phone

Circuit Diagram of RF Block (Version 04.27 Edit 105)

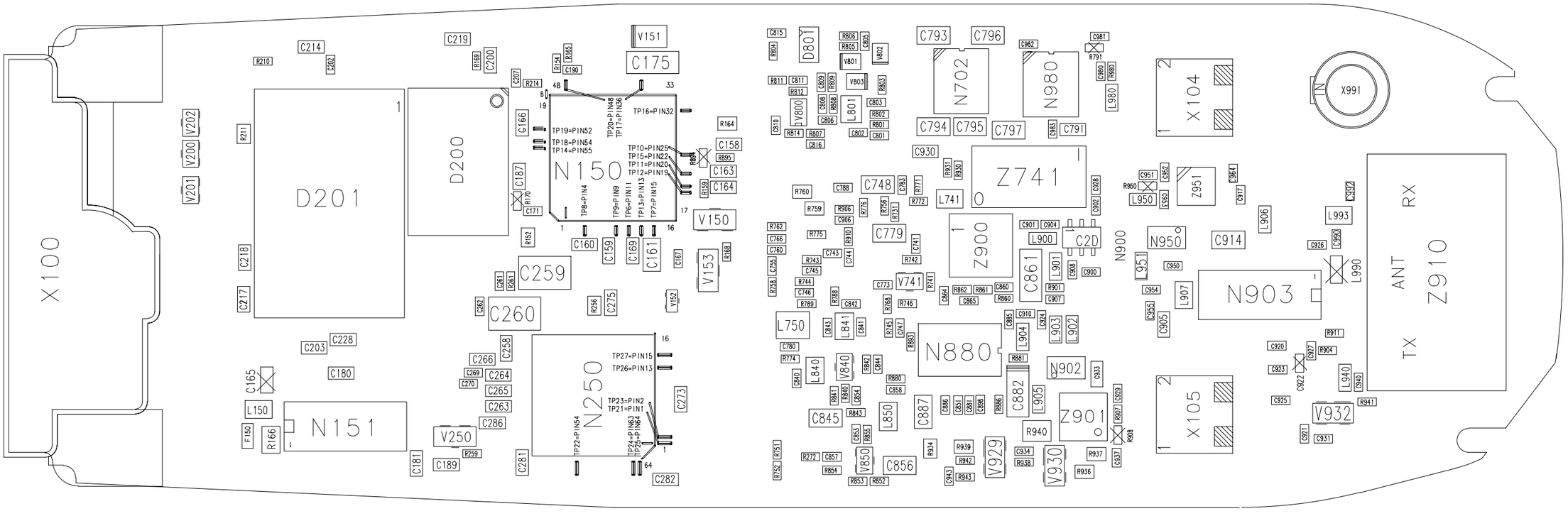


Layout Diagram of UT4S



testpoint	name	condition	dc–level	ac–level
J200		Only for R&D use		
J201		Only for R&D use		
J202		Only for R&D use		
J203		Only for R&D use		
TP1, D202 pin 78	HOOKINT	Remote controlheadset	pulse active 2.8 V, non–active 0 V	
TP2, D202 pin 77	HEADSETINT	Headset connected	pulse active 0 V, non–active 2.8 V	
TP3, D202 pin 117	TXF	False transmission indicator	Irregular from 0 V to 2.8 V	
TP4, R153	RSENSE	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP5, R153	VOUT	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP30, G850 pin 3	VCTCXO	power on		typ. 0.8 V – 1.2 Vpp sinewave 19.44 MHz
TP31, G820 pin 3	CTL	active state ch 300	typ. 2.2 V	
TP32, G860 pin 3	CTL	active state ch 1000	typ. 2.2 V	

Layout Diagram of UT4S

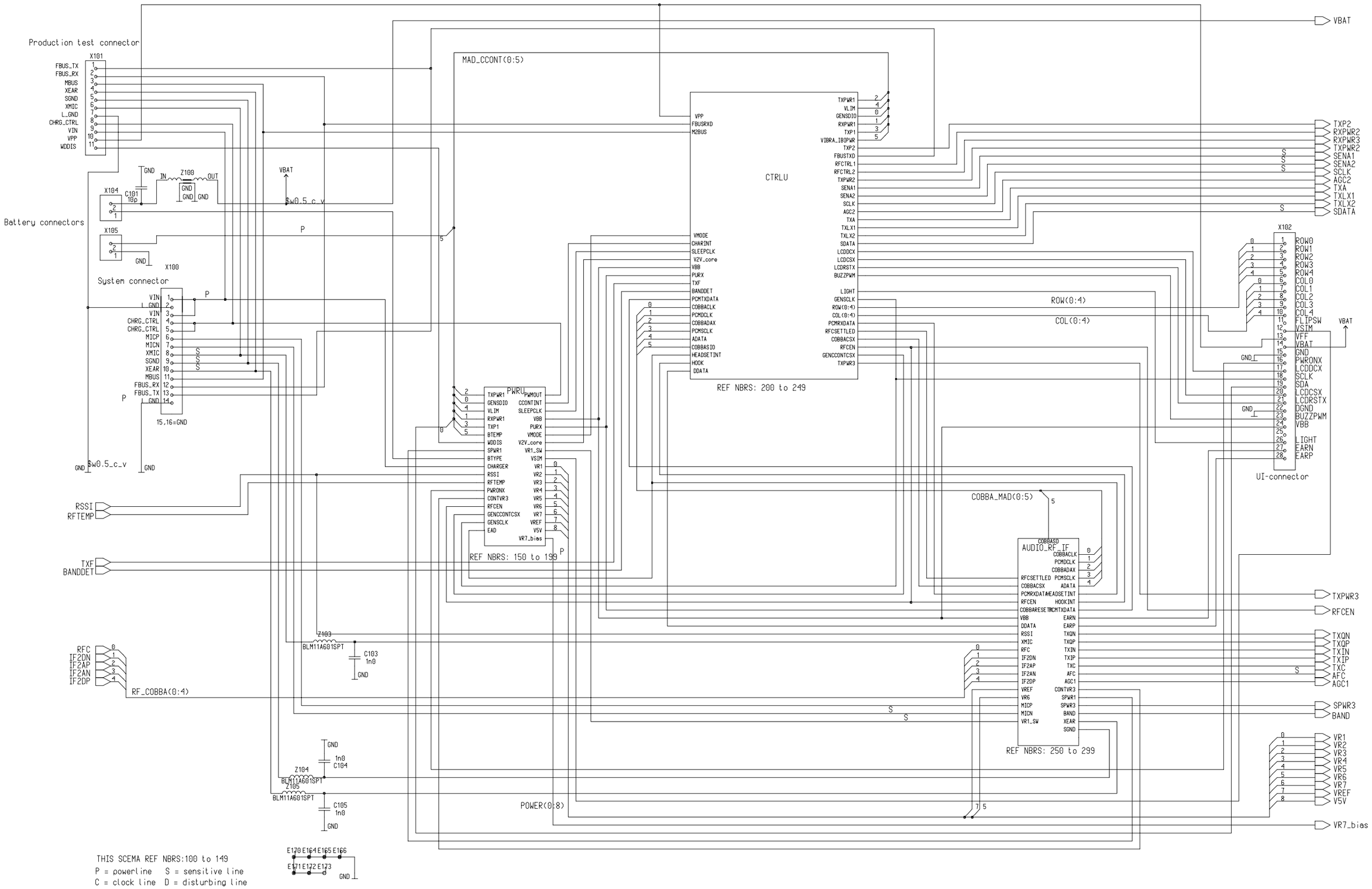


testpoint	name	condition	dc–level	ac–level
TP6, N150 pin 11	VR5	supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP7, N150 pin 15	VR4	regulated supply for RX	2.8 V min 2.7 V / max 2.85 V	
TP8, N150 pin 4	VR3	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP9, N150 pin 9	VR2	regulated supply for SYNT	2.8 V min 2.7 V / max 2.85 V	
TP10, N150 pin 25	VR1	regulated supply for VCTCXO	2.8 V min 2.7 V / max 2.85 V	
TP11, N150 pin 20	VR7	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP12, N150 pin 19	VR7BASE	VR7 regulator external transistor base current	2.8 V min 2.7 V / max 2.85 V	
TP13, N150 pin 13	VREF	ref.voltage for N150	1.5 V +/– 1.5%	
TP14, N150 pin 55	VBB	regulated supply for BaseBand	2.8 V min 2.7 V / max 2.85 V	
TP15, N150 pin 22	VR6	regulated supply for COBBA	2.8 V min 2.7 V / max 2.85 V	
TP16, N150 pin 32	V5V	regulated supply to 2GHz PLL	5.0 V min 4.8 V / max 5.2 V	
TP17, N150 pin 36	VSIM	regulated supply for flashing	3.0 V min 2.8 V / max 3.2 V	
TP18, N150 pin 54	PURX	RESET Power up/down	reset state 0 V, normal state 2.8 V	

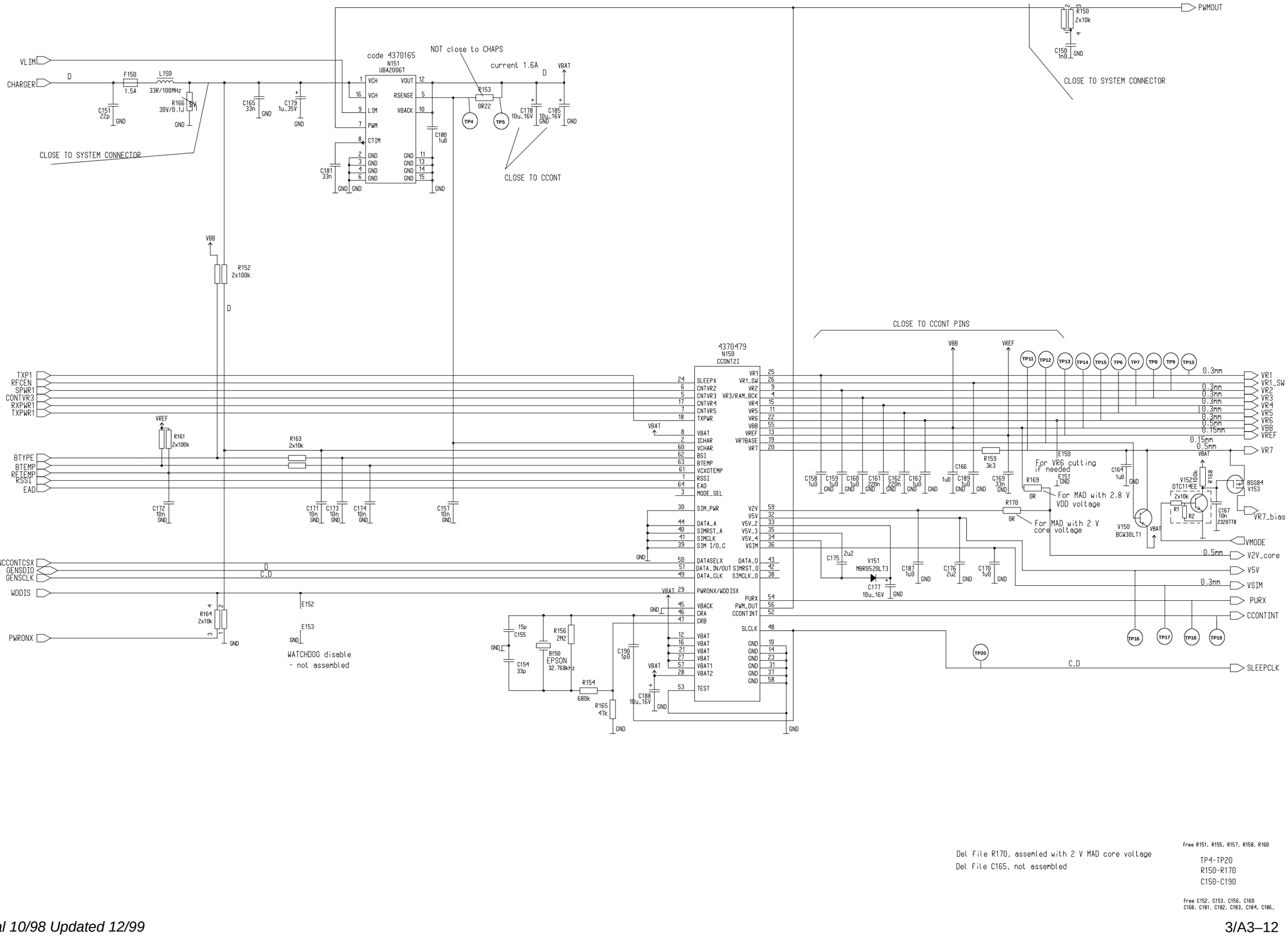
testpoint	name	condition/type	dc–level	ac–level
TP19, N150 pin 52	CCON-TINT	Charger interrupt	pulse active 2.8 V, non–active 0 V	
TP20, N150 pin 48	SLCLK	32.768 kHz, power on	pulsed DC (0V/2.8 V)	
TP21, N250 pin 1	RFCEN	active state	pulse active 2.8 V, non–active 0 V	
TP22, N250 pin 54	RFCSETTLED	active state	pulse active 2.8 V, non–active 0 V	
TP23, N250 pin 2	RFC	19.44 MHz sinewave		0.2Vpp–1V pp sine-wave
TP24, N250 pin 63	COB-BACLK	9.72 MHz, active state	pulsed DC (0V/2.8V)	
TP25, N250 pin 64	ADATA	active state	pulsed DC (0V/2.8V)	
TP26, N250 pin 13	AFC	Autom.Freq.control	0 – 2.3 V, typ. 1.15 V (room temp)	
TP27, N250 pin 15	TXC	TX power control voltage	@level 10 typ.ca 0.5 V pulse @level 2 typ.ca 1.7 V pulse	
TP33, R939	DETO	active state	0.4 V – 2.2 V	
TP34, R220	VAPC	active state	0 V – 1.5 V typ.	
TP35, N702 pins 9,11,12.13,14	VR8 – VR 12	power on	nominal 2.8 V	

[]

Circuit Diagram of System Blocks (Version 04.72 Edit 11)



Circuit Diagram of Power Supply (Version 04.72 Edit 8)



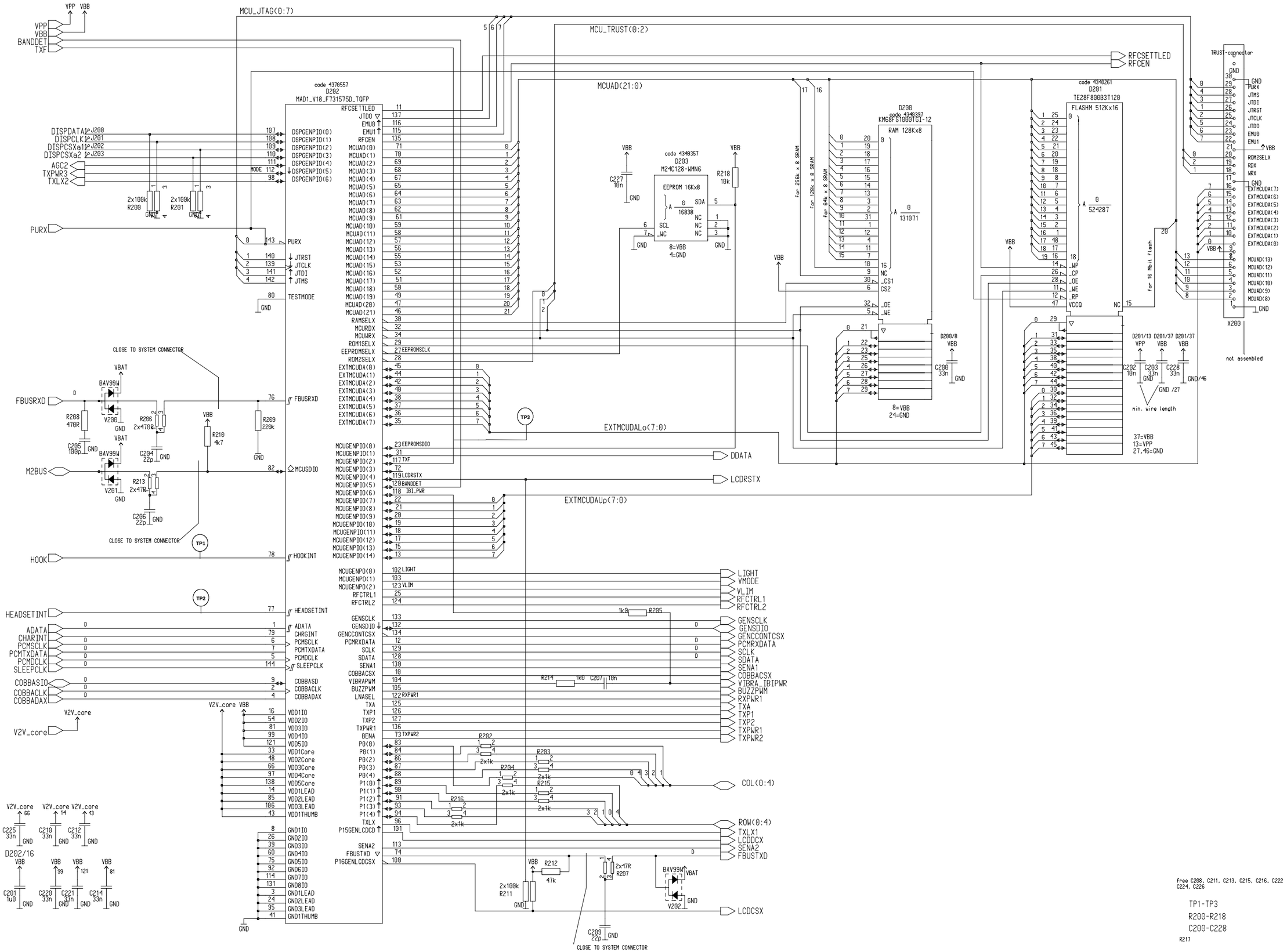
Del file R170, assemled with 2 V MAD core voltage
Del file C165, not assembled

Free R151, R155, R157, R158, R160

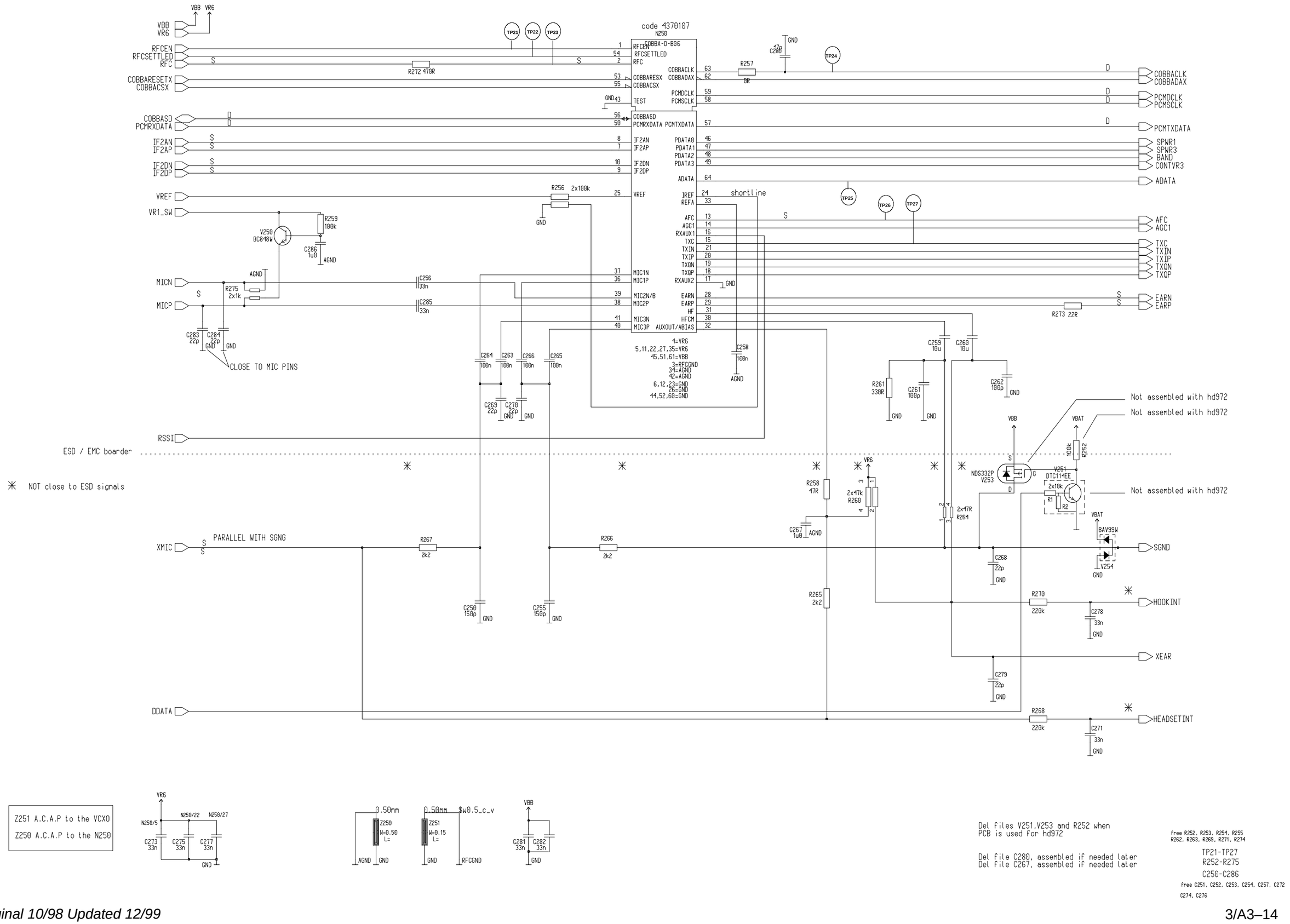
TP4-TP20
R150-R170
C150-C190

Free C152, C153, C156, C160
C168, C181, C182, C183, C184, C186,

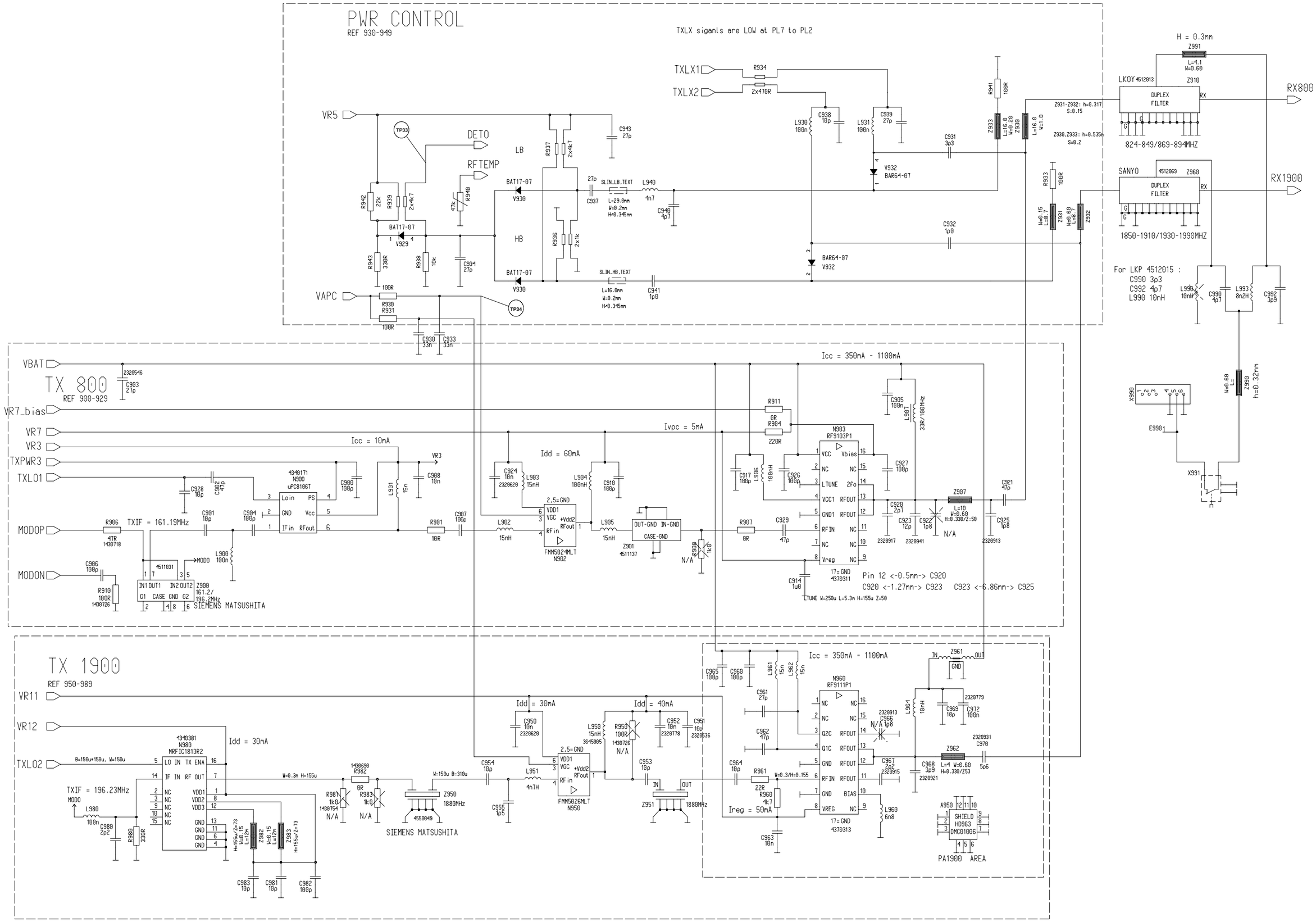
Circuit Diagram of CTRLU Block (Version 04.72 Edit 9)



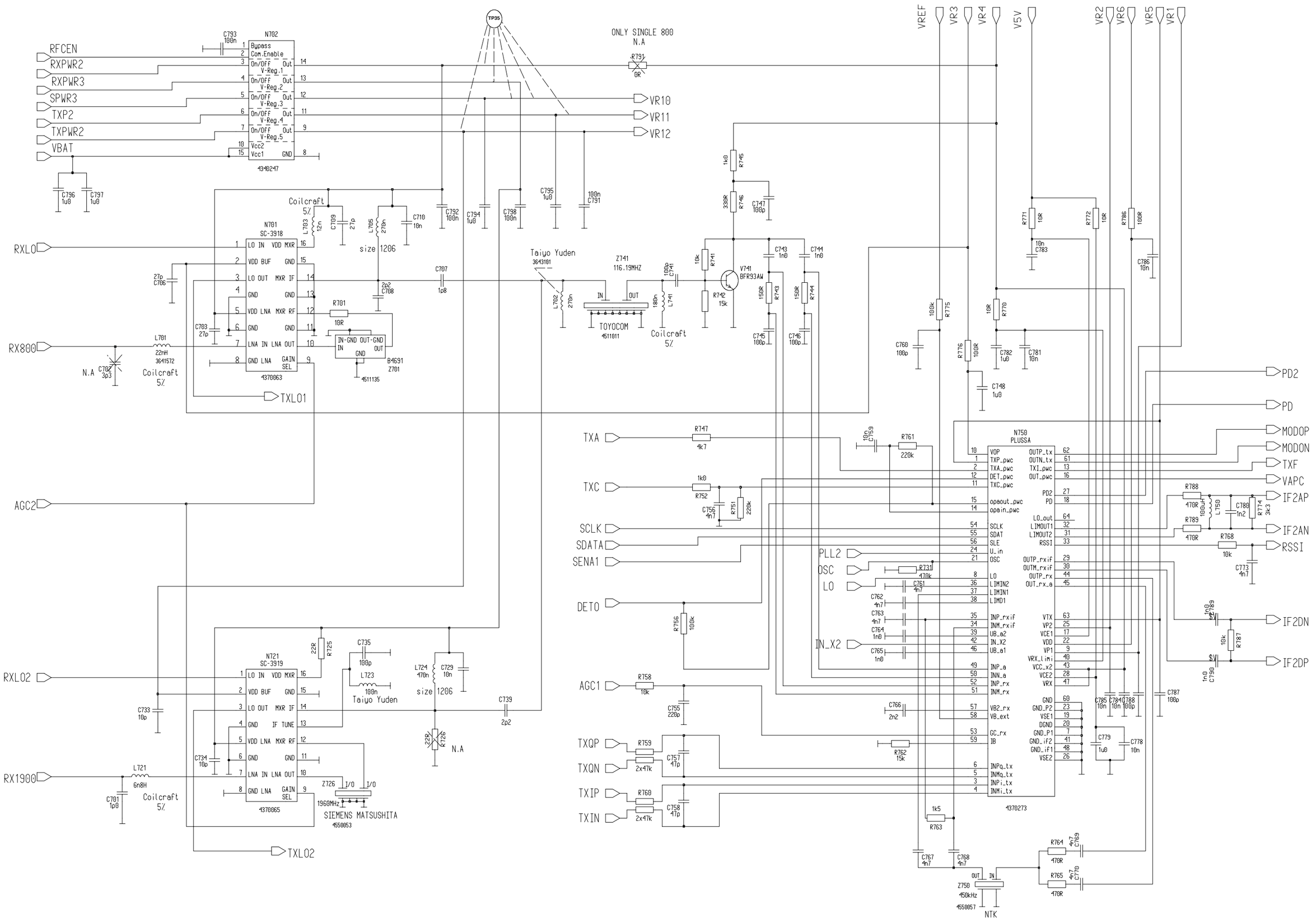
Circuit Diagram of Audio (Version 04.72 Edit 7)



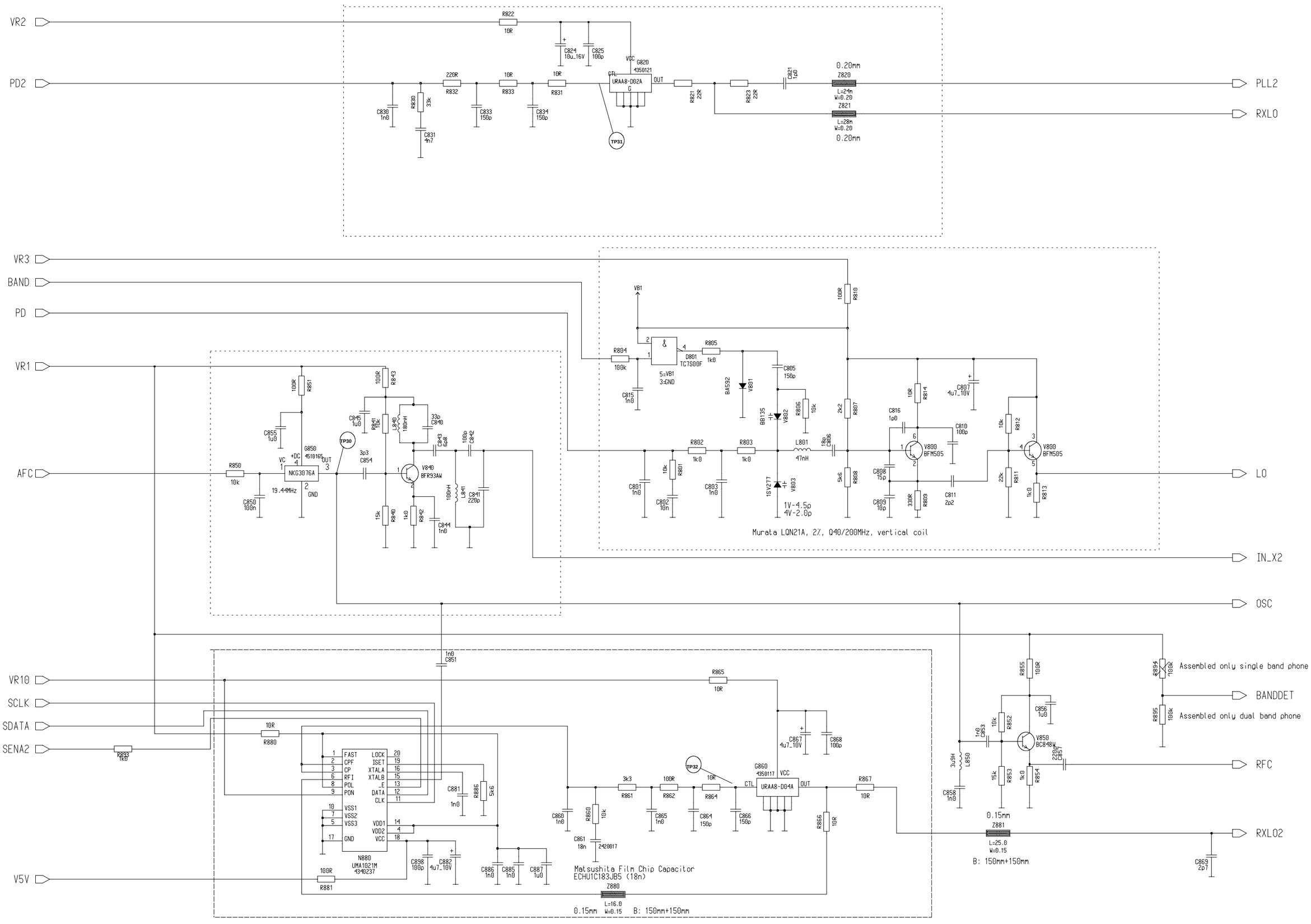
Circuit Diagram of Transmitter (Version 04.72 Edit 8)



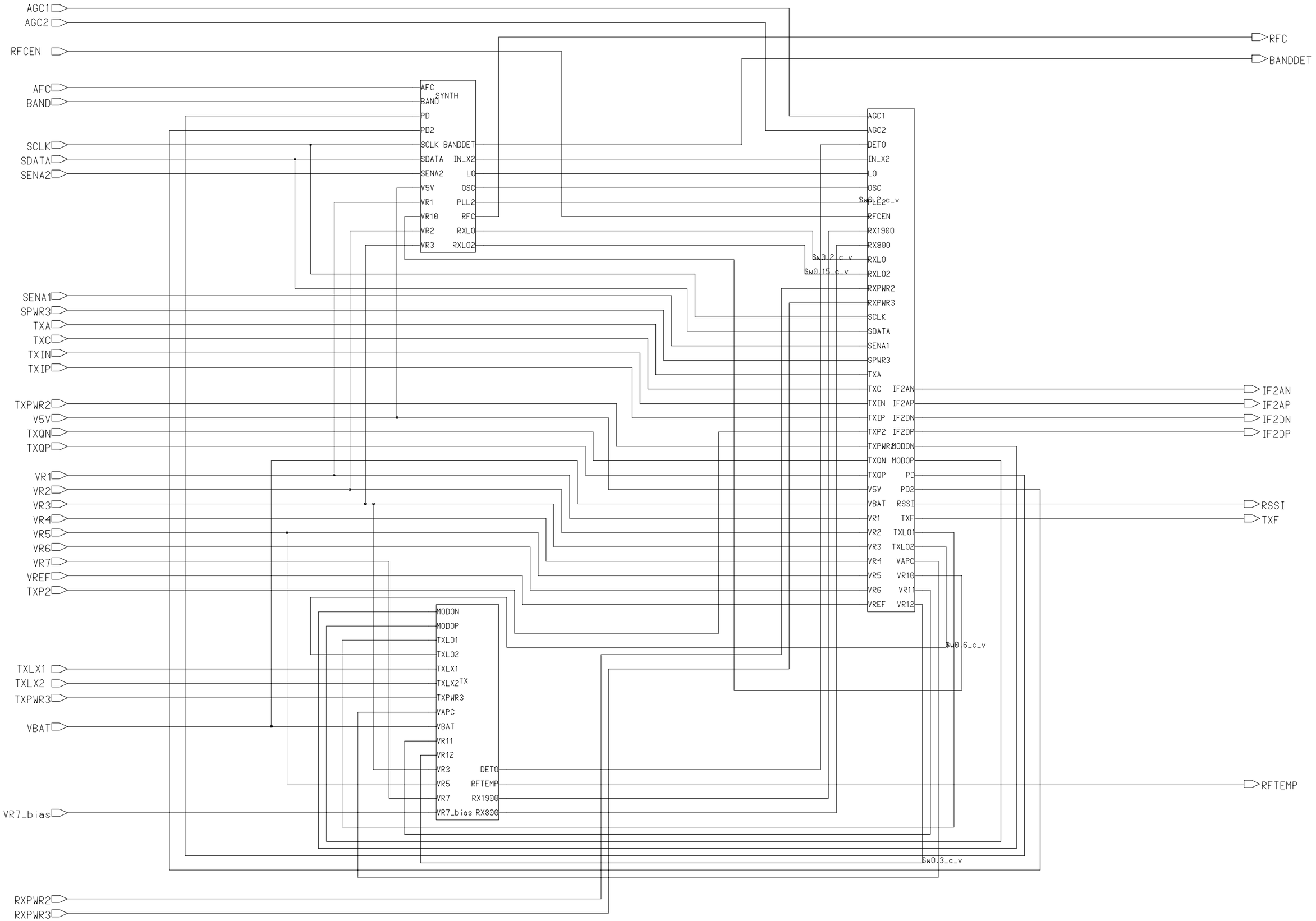
Circuit Diagram of Receiver (Version 04.72 Edit 8)



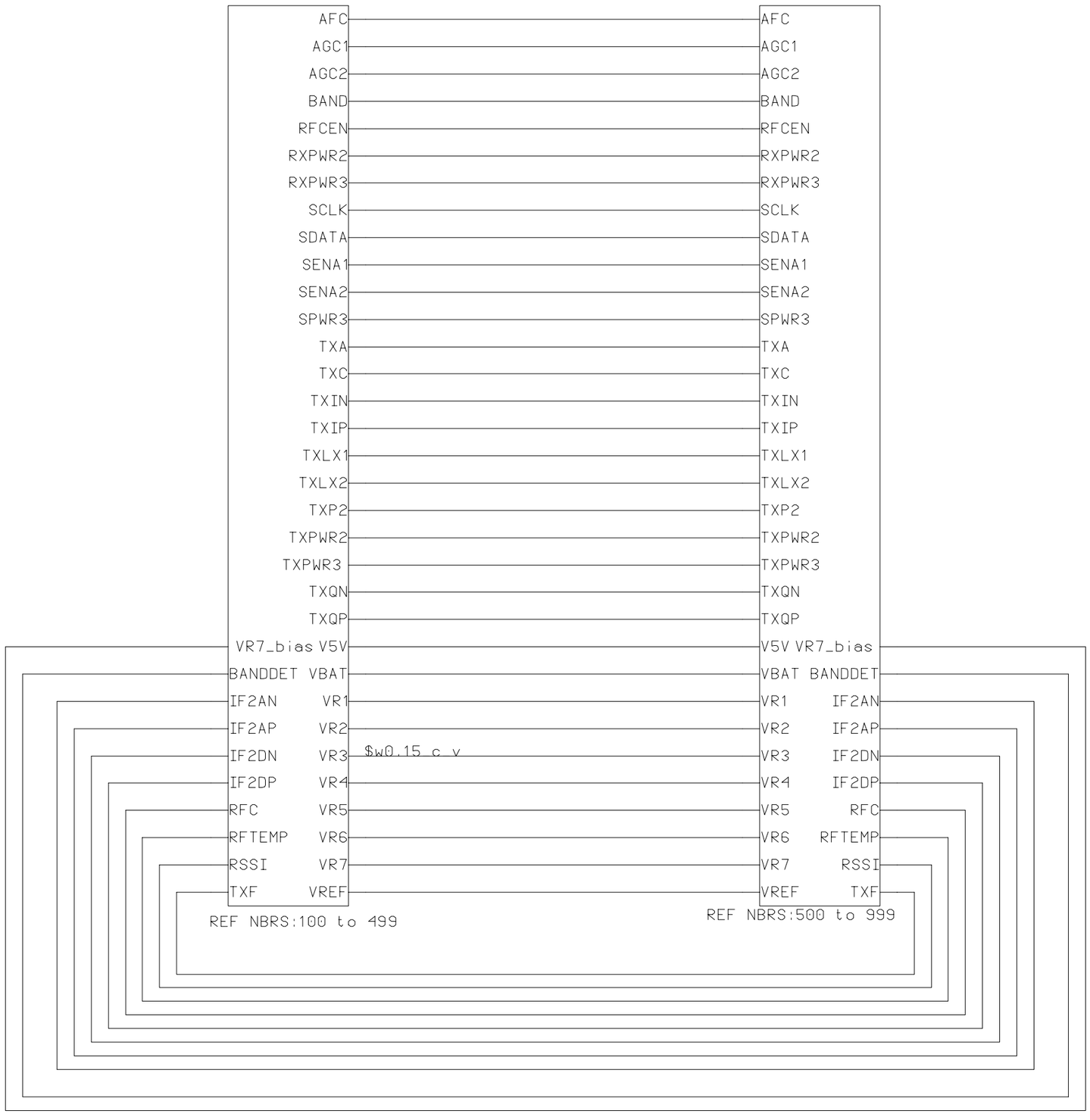
Circuit Diagram of Synthesizer (Version 04.72 Edit 6)



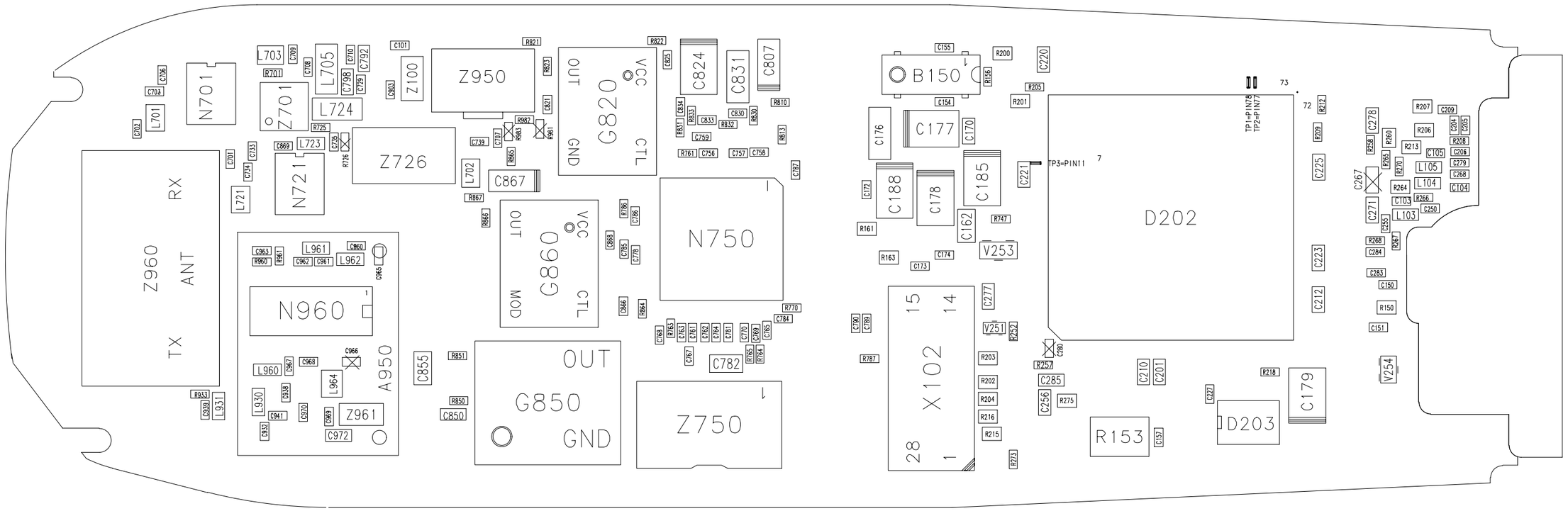
Circuit Diagram of RF Block (Version 04.72 Edit 5)



Circuit Diagram of RF–BB Interface (Version 04.72 Edit 8)

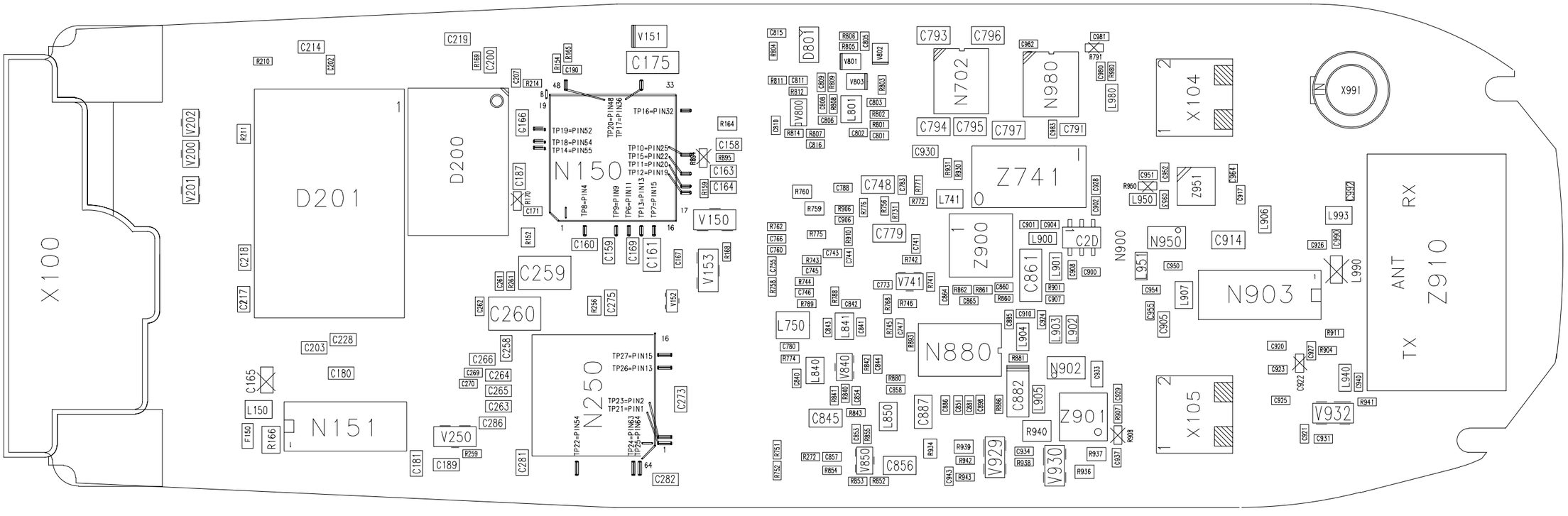


Layout Diagram of UT4S



testpoint	name	condition	dc–level	ac–level
J200		Only for R&D use		
J201		Only for R&D use		
J202		Only for R&D use		
J203		Only for R&D use		
TP1, D202 pin 78	HOOKINT	Remote controlheadset	pulse active 2.8 V, non–active 0 V	
TP2, D202 pin 77	HEADSETINT	Headset connected	pulse active 0 V, non–active 2.8 V	
TP3, D202 pin 117	TXF	False transmission indicator	Irregular from 0 V to 2.8 V	
TP4, R153	RSENSE	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP5, R153	VOUT	VOUT detection	min 0V, typ 3.6 V, max 5.2 V	
TP30, G850 pin 3	VCTCXO	power on		typ. 0.8 V – 1.2 Vpp sinewave 19.44 MHz
TP31, G820 pin 3	CTL	active state ch 300	typ. 2.2 V	
TP32, G860 pin 3	CTL	active state ch 1000	typ. 2.2 V	

Layout Diagram of UT4S



testpoint	name	condition	dc–level	ac–level
TP6, N150 pin 11	VR5	supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP7, N150 pin 15	VR4	regulated supply for RX	2.8 V min 2.7 V / max 2.85 V	
TP8, N150 pin 4	VR3	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP9, N150 pin 9	VR2	regulated supply for SYNT	2.8 V min 2.7 V / max 2.85 V	
TP10, N150 pin 25	VR1	regulated supply for VCTCXO	2.8 V min 2.7 V / max 2.85 V	
TP11, N150 pin 20	VR7	regulated supply for TX	2.8 V min 2.7 V / max 2.85 V	
TP12, N150 pin 19	VR7BASE	VR7 regulator external transistor base current	2.8 V min 2.7 V / max 2.85 V	
TP13, N150 pin 13	VREF	ref.voltage for N150	1.5 V +/– 1.5%	
TP14, N150 pin 55	VBB	regulated supply for BaseBand	2.8 V min 2.7 V / max 2.85 V	
TP15, N150 pin 22	VR6	regulated supply for COBBA	2.8 V min 2.7 V / max 2.85 V	
TP16, N150 pin 32	V5V	regulated supply to 2GHz PLL	5.0 V min 4.8 V / max 5.2 V	
TP17, N150 pin 36	VSIM	regulated supply for flashing	3.0 V min 2.8 V / max 3.2 V	
TP18, N150 pin 54	PURX	RESET Power up/down	reset state 0 V, normal state 2.8 V	

testpoint	name	condition/type	dc–level	ac–level
TP19, N150 pin 52	CCON-TINT	Charger interrupt	pulse active 2.8 V, non–active 0 V	
TP20, N150 pin 48	SLCLK	32.768 kHz, power on	pulsed DC (0V/2.8 V)	
TP21, N250 pin 1	RFCEN	active state	pulse active 2.8 V, non–active 0 V	
TP22, N250 pin 54	RFCSETTLED	active state	pulse active 2.8 V, non–active 0 V	
TP23, N250 pin 2	RFC	19.44 MHz sinewave		0.2Vpp–1V pp sine-wave
TP24, N250 pin 63	COB-BACLK	9.72 MHz, active state	pulsed DC (0V/2.8V)	
TP25, N250 pin 64	ADATA	active state	pulsed DC (0V/2.8V)	
TP26, N250 pin 13	AFC	Autom.Freq.control	0 – 2.3 V, typ. 1.15 V (room temp)	
TP27, N250 pin 15	TXC	TX power control voltage	@level 10 typ.ca 0.5 V pulse @level 2 typ.ca 1.7 V pulse	
TP33, R939	DETO	active state	0.4 V – 2.2 V	
TP34, R220	VAPC	active state	0 V – 1.5 V typ.	
TP35, N702 pins 9,11,12.13,14	VR8 – VR 12	power on	nominal 2.8 V	